Amendments to the Specification

Please replace the paragraph beginning at page 3, line 9, with the following replacement paragraph:

In this case, the increase of the dopants concentration of well causes a generation of the junction capacitance in the source/drain region, and the junction capacitance causes a delay of gate signal, which functions to reduce reliability of the semiconductor device. Particularly, these are ~~one~~ some of the problems to be solved in conjunction with the tendency of gradual increase of degradation of device characteristics due to a short channel effect according to a gradual reduction of critical dimensions of the gate electrode.

Please replace the paragraph beginning at page 4, line 4, with the following replacement paragraph:

In order to accomplish this object, there is provided a method for fabricating MOS transistors, the method comprising the steps of: forming a buffer oxide layer on a semiconductor substrate having an isolation layer; successively conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer; removing the buffer oxide layer; forming a sacrificial layer ~~of~~ on the semiconductor substrate; patterning the sacrificial layer to form a trench defining a gate electrode forming region; successively conducting ion implantations for threshold voltage adjustment and punch stop formation on the semiconductor substrate area exposed by the trench; forming a gate oxide layer on the surface of the substrate under the bottom face of the trench; forming a polysilicon layer on the sacrificial layer so as to completely bury the trench; polishing the polysilicon layer until the surface of the sacrificial layer is exposed, so as to form a gate electrode; removing the sacrificial layer; forming an LDD region in the surface of the substrate at both side portions of the gate electrode; forming spacers on both side walls of the gate

electrode; and forming the source/drain regions in the surface of the substrate at both side portions of the gate electrode including the spacers.

Please replace the paragraph beginning at page 6, line 18, with the following replacement paragraph:

Referring to the FIG. 2B, the buffer oxide layer is removed and a sacrificial layer 27 composed of a chemical vapor deposition (CVD) oxide layer is formed on the semiconductor substrate 21 so as to have a thickness ranging for example between ~~500~~ 500Å and ~~1000~~1000Å, corresponding to a desired thickness of a gate electrode. Then, the sacrificial layer 27 is patterned to form a trench 29 defining a gate electrode forming region according a conventional photolithography process. In this case, the patterning of the sacrificial layer is implemented by wet-etching process. Then, ion implantations for threshold voltage adjustment and punch stop formation are successively implemented only on an area of the semiconductor substrate 21, i.e., a channel formation region of MOS transistor. As a result, ion implantation for ~~field~~ punch stop formation is conducted only under the to-be-gate electrode area. The impurity for well formation and field stop formation is boron or phosphorous or Arsenic. ~~Implant is~~ Implants are made at a sufficient energy to form a specific region, for example, barriers below the source /drain junction for well and field stop or threshold voltage adjustment and punch stop.

Please replace the paragraph beginning at page 7, line 16, with the following replacement paragraph:

Referring to the FIG. 2C, a gate oxide layer 31a is formed on the surface of the substrate 21 ~~under~~ at the bottom face of the trench 29 using an oxidation process, and a polysilicon layer 31b is formed on the sacrificial layer 27 so as to completely ~~bury~~ fill the trench 29.